INTEGRATED CIRCUITS

DATA SHEET

TDA4881
Advanced monitor video controller

Preliminary specification
File under Integrated Circuits, IC02

November 1992

Philips Semiconductors

PHILIPS

Advanced monitor video controller TDA4881

FEATURES

- Fully DC controllable
- 3 separate video channels
- Input black level clamping
- White level adjustment for 2 channels only
- Brightness control with correct grey scale tracking
- Contrast control for all 3 channels simultaneously
- Cathode feedback to internal reference for cut-off control, which allows unstabilized video supply voltage
- Current outputs for RGB signal currents
- RGB voltage outputs to external peaking circuits
- Blanking and switch-off input for screen protection
- Sync on green operation possible

GENERAL DESCRIPTION

The TDA4881 is a monolithic integrated RGB amplifier for colour monitor systems with super VGA performance, intended for DC or AC coupling of the colour signals to the cathodes of the CRT. With special advantages the circuit can be used in conjunction with the TDA4851.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage (pin 7)		7.2	8.0	8.8	V
I_P	supply current		–	46	56	mA
$V_{I(b-w)}$	input voltage (black-to-white, pins 2, 5 and 8)		–	0.7	1.0	V
$V_{O(b-w)}$	output voltage (black-to-white, pins 19, 16 and 13)	nominal contrast and nominal gain	–	0.8	–	V
$I_{O(b-w)}$	output current (black-to-white, pins 20, 17 and 14)		–	50	–	mA
I_M	peak output current (pins 20, 17 and 14)		–	–	100	mA
B	bandwidth	–3 dB	70	–	–	MHz
G_{nom}	nominal gain		–	1	–	dB
G_v	gain control range for 2 channels (relative to G_{nom})		–4	–	+2	dB
C_v	contrast control range (relative to G_{nom})		–20	–	+3	dB
ΔV_{bl}	brightness control range	nominal gain	–80	–	+240	mV
T_{amb}	operating ambient temperature range		0	–	+70	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA4881	20	DIL	plastic	SOT146[(1)]

Note

1. SOT146-1; 1996 November 27.

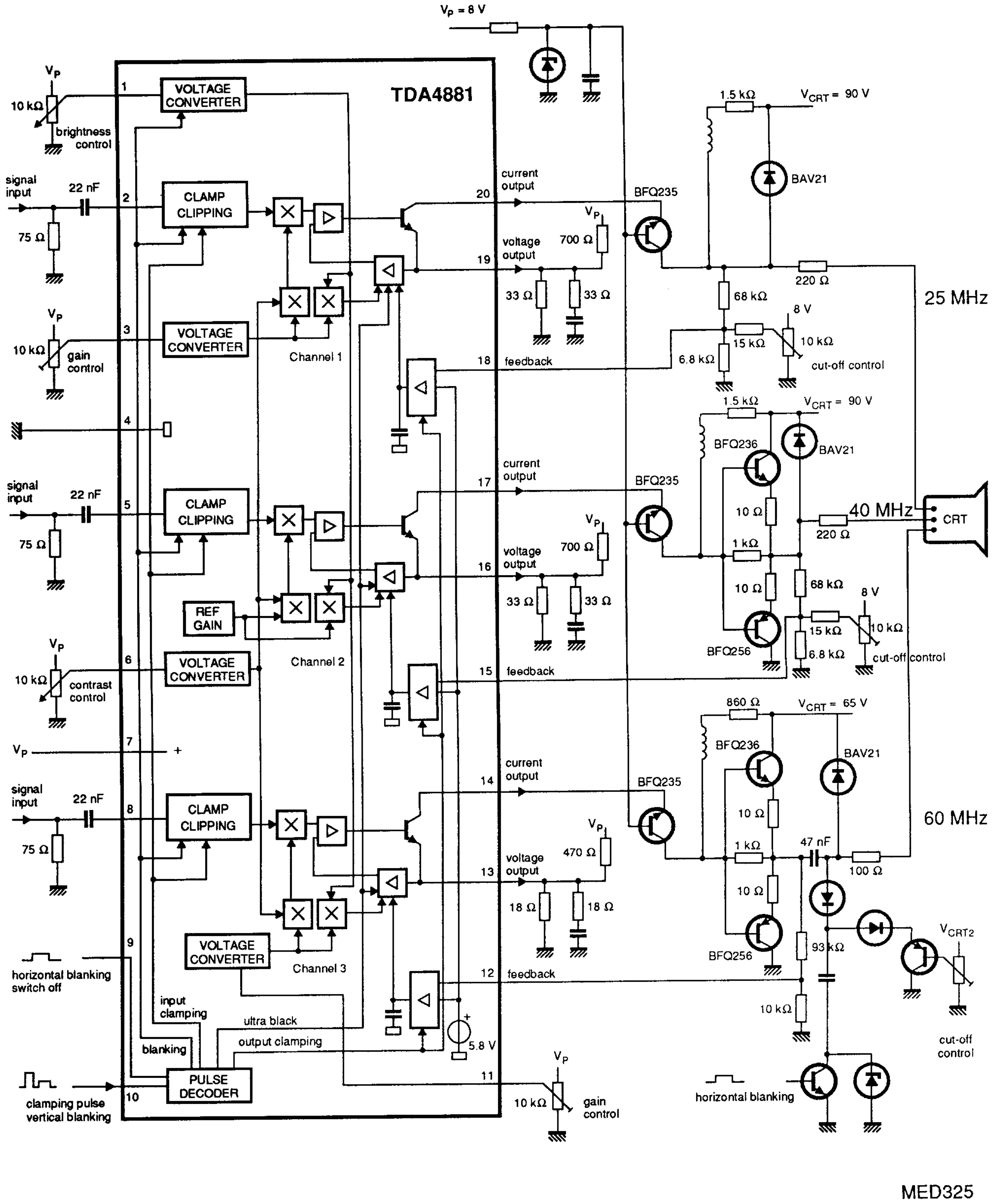


Fig.1 Block diagram and basic application circuit for DC and AC coupling.

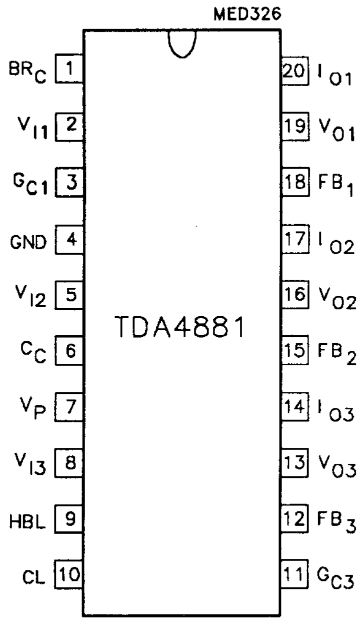


Fig.2 Pin configuration

PINNING

SYMBOL	PIN	DESCRIPTION
BR_C	1	brightness control
V_{I1}	2	signal input Channel 1
G_{C1}	3	gain control Channel 1
GND	4	ground
V_{I2}	5	signal input Channel 2
C_C	6	contrast control
V_P	7	supply voltage
V_{I3}	8	signal input Channel 3
HBL	9	horizontal blanking, switch off
CL	10	input clamping, vertical blanking
G_{C3}	11	gain control Channel 3
FB_3	12	feedback Channel 3
V_{O3}	13	voltage output Channel 3
I_{O3}	14	current output Channel 3
FB_2	15	feedback Channel 2
V_{O2}	16	voltage output Channel 2
I_{O2}	17	current output Channel 2
FB_1	18	feedback Channel 1
V_{O1}	19	voltage output Channel 1
I_{O1}	20	current output Channel 1

FUNCTIONAL DESCRIPTION

RGB input signals (0.7 $V_{(p-p)}$) are capacitively coupled into the TDA4881 (pins 2, 5 and 8) from a low ohmic source and are clamped to an internal DC voltage (artificial black level). Composite signals will not disturb normal operations because an internal clipping circuit cuts all signal parts below black level. Channels 1 and 3 have a maximum total voltage gain of 6 dB (maximum contrast and maximum individual channel gain), Channel 2 of 4 dB (maximum contrast and nominal channel gain). With the nominal channel gain of 1 dB and nominal contrast setting the nominal black-to-white output amplitude is 0.8 $V_{(p-p)}$. DC voltages are used for brightness, contrast and gain control.

Brightness control yields a simultaneous signal black level shift of the three channels relative to a reference black level. For nominal brightness (pin 1 open-circuit) the signal black level is equal to the reference black level.

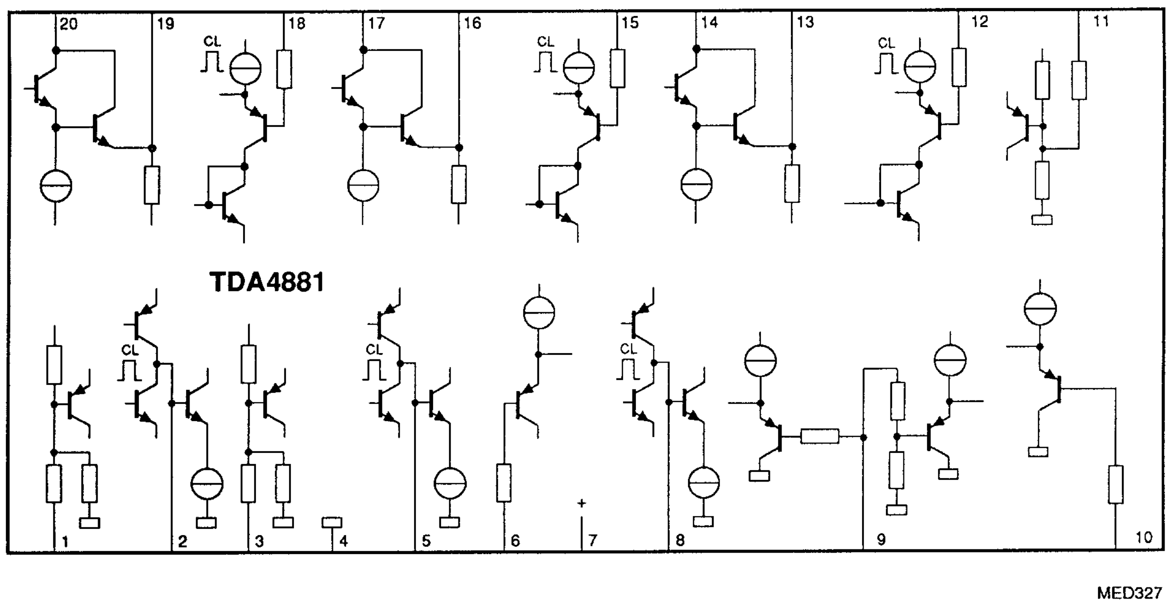
Contrast control is achieved by a voltage at pin 6 and affects the three channels simultaneously.
To provide the correct white point, an individual *gain control* (pins 3 and 11) adjusts the signals of Channels 1 and 3 compared to the reference Channel 2. Gain setting effects contrast and brightness to achieve correct grey scale tracking. Each *output stage* provides a current output (pins 20, 17 and 14) and a voltage output (pins 19, 16 and 13). External cascode transistors reduce power consumption of the IC and prevent breakdown of the output transistors. Signal output currents and peaking characteristics are determined by external components at the voltage outputs and the video supply. The three channels have separate internal feedback loops which ensure large signal linearity and marginal signal distortion in spite of output transistor thermal V_{BE} variation.

The *clamping pulse* (pin 10) is used for *input clamping* only. The input signals have to be at black level during the clamping pulse and are clamped to an internal artificial black level. The coupling capacitors are used in this way for black level storage. Because the threshold for the clamping pulse is higher than that for vertical blanking (pin 10) the rise and fall times of the clamping pulse have to be faster than 75 ns/V (1 V to 3.5 V).

The *vertical blanking pulse* will be detected if the input voltage (pin 10) is higher than the threshold voltage for approximately 300 ns but does not exceed the threshold for the clamping pulse in the time between. During the vertical blanking pulse the input clamping is disabled to avoid misclamping in the event of composite input signals. The input signal is blanked and the artificial black level is inserted instead. Additionally the brightness is internally set to its nominal value, thus the output signal is at reference black level. The DC value of the reference black level will be adjusted by cut-off stabilization.

During *horizontal blanking* (pin 9) the output signal is set to reference black level as previously described and *output clamping* is activated. If the voltage at pin 9 exceeds the *switch off* threshold the signal is blanked and switched to ultra black level for screen protection and spot suppression during V-flyback. Ultra black level is the lowest possible output voltage (at voltage outputs) and does not depend on cut-off stabilization.

For *cut-off stabilization* (DC coupling to the CRT) respectively *black level stabilization* (AC coupling) the video signal at the cathode or the coupling capacitor is divided by an adjustable voltage divider and fed to the feedback inputs (pins 18, 15 and 12). During horizontal blanking time this signal is compared with an internal DC voltage of approximately 5.8 V. Any difference will lead to a reference black level correction by charging or discharging the integrated capacitor which stores the reference black level information between the horizontal blanking pulses.



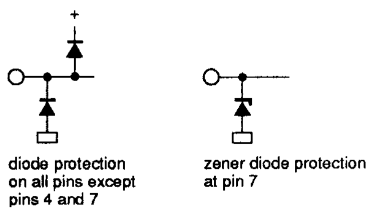


Fig.3 Internal circuits.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage (pin 7)	0	8.8	V
V_i	input voltage range (pins 2, 5 and 8)	–0.1	V_P	V
V_{ext}	external DC voltage ranges			
	pins 20, 17 and 14	–0.1	V_P	V
	pins 19, 16 and 13	no external voltages		
	pins 1, 3, 6 and 11	–0.1	V_P	V
	pin 9	–0.1	V_P+0.7	V
	pin 10	–0.7	V_P +0.7	V
I_o	average output current (pins 20, 17 and 14)	0	50	mA
I_M	peak output current (pins 20, 17 and 14)	0	100	mA
P_{tot}	total power dissipation	–	1200	mW
T_{stg}	storage temperature range	–25	+150	°C
T_{amb}	operating ambient temperature range	0	+70	°C
T_j	junction temperature	–25	+150	°C
V_{ESD}	electrostatic handling for all pins (note 1)	–500	+500	V

Note to the Limiting Values

1. Equivalent to discharging a 200 pF capacitor through a 0 Ω series resistor.

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	65 K/W

CHARACTERISTICS

V_P = 8.0 V, T_{amb} = +25 °C; all voltages measured to GND (pin 4); unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range (pin 7)		7.2	8.0	8.8	V
I_P	supply current (pin 7)		–	46	56	mA
Video signal inputs						
$V_{I(b-w)}$	input voltage (black-to-white, pins 2, 5 and 8)		–	0.7	1.0	V
$I_{2, 5, 8}$	DC current	no clamping	–0.1	–	0.1	µA
		during clamping	±50	–	–	µA
Brightness control						
V_1	input voltage range	see note 1	1.0	–	6.0	V
R_1	input resistance to V_{N1}		–	50	–	kΩ
ΔV_{bl1}	black level voltage change at nominal gain (pins 19, 16 and 13)	V_1 = 1.0 V; $V_{3, 11}$ open-circuit	–	–80	–	mV
		V_1 = 6.0 V; $V_{3, 11}$ open-circuit	–	240	–	mV
V_{N1}	input voltage for nominal brightness	pin 1 open-circuit	–	2.25	–	V
Contrast control (see note 2)						
V_6	input voltage range	see note 1	1.0	–	6.0	V
I_6	current		–5	–1	–	µA
C_v	contrast relative to nominal contrast	V_6 = 6.0 V; $V_{3, 11}$ open-circuit	–	3	–	dB
		V_6 = 4.5 V; $V_{3, 11}$ open-circuit	–	0	–	dB
		V_6 = 1.0 V; $V_{3, 11}$ open-circuit	–	–20	–	dB
Tr	tracking of RGB signals	2.5 V < V_6 < 6 V; $V_{3, 11}$ open-circuit	–	0	0.5	dB
Gain control						
$V_{3, 11}$	input voltage range	see note 1	1.0	–	6.0	V
$R_{3, 11}$	input resistance against $V_{N3, N11}$		–	43	–	kΩ
G_v	gain relative to nominal gain	V_6 = 4.5 V; $V_{3, 11}$ = 6 V	–	2	–	dB
		V_6 = 4.5 V; $V_{3, 11}$ = 1 V	–	–4	–	dB
$V_{N3, N11}$	input voltage for nominal gain	pin 3, 11 open-circuit	–	4.6	–	V
Feedback input						
V_{int}	internal reference voltage	see note 3	tbn	5.8	tbn	V
$I_{18, 15, 12}$	output current	during output clamping	–1.5	–1.0	–0.1	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Voltage outputs (pins 19, 16 and 13)						
$V_{O(b-w)}$	signal output voltage (black-to-white value)	$V_{3, 11}$ open; V_6 = 4.5 V; $V_{I(b-w)}$ = 0.7 V	–	0.8	–	V
V_{bl}	black level voltage	during output clamping; depending on black level adjustment; see note 4	0.3	–	1.0	V
		during switch-off	–	0.1	0.3	V
S/N	signal-to-noise ratio	see note 5	–	–	44	dB
Frequency response at voltage outputs						
G_{vf}	gain decrease by frequency response at pins 19, 16 and 13	70 MHz	–	–	–3	dB
t_{rO}	rise time at voltage output (pins 19, 16 and 13)	10% to 90% amplitude; input rise time = 1 ns	–	4.5	5.0	ns
Current outputs (pins 20, 17 and 14)						
$I_{O(b-w)}$	signal current (black-to-white)		–	50	–	mA
		with peaking; see note 6	–	–	100	mA
$V_{20-19, 17-16, 14-13}$	HF saturation of output transistors	I_O = 50 mA	–	–	2.0	V
		I_O = 100 mA	–	–	2.2	V
Threshold voltages (see note 7)						
V_9	threshold for horizontal blanking (blanking, output clamping)		1.2	1.4	1.6	V
	threshold for switch-off (blanking, minimum black level, no output clamping)		5.8	6.5	6.8	V
R_9	input resistance referenced to ground		50	80	110	kΩ
t_{d9}	delay between horizontal blanking input and output signal blanking		–	35	60	ns
V_{10}	threshold for vertical blanking (blanking, no input clamping)	see Fig.4	1.2	1.4	1.6	V
	threshold for clamping (input clamping, no blanking)	see Fig.4	2.6	3.0	3.5	V
I_{10}	input current		–3	–1	–	µA
$t_{r,f10}$	rise and fall time for clamping pulse	transition 1 to 3.5 V; see Fig.4	–	–	75	ns/V
t_{w10}	clamping pulse width	V_{10} = 3 V	0.6	–	–	µs
t_{d10}	delay between vertical blanking input and output signal blanking	see Fig.4	–	300	–	ns

Notes to the characteristics

1. Typical range is 1 to 6 V, the range can be increased (e.g. 0 to 7 V) to slightly increase the control range.
2. Open contrast control pin leads to undefined contrast setting.
3. The internal reference voltage can be measured at pins 18, 15 and 12 during output clamping in closed feedback loop.
4. Minimum guaranteed control range, the typical minimum black level voltage is 0.1 V.
5. The signal-to-noise ratio is calculated by the formula (frequency range 1 to 70 MHz):

$$\frac{\text{peak-to-peak value of the nominal signal output voltage}}{\text{RMS value of the noise output voltage}}$$

6. The external RC combinations at pins 19, 16 and 13 enables peak currents during transients.
7. The internal threshold voltages are derived from an internally stabilized voltage. The internal pulses are generated if the input pulses are higher than the thresholds.

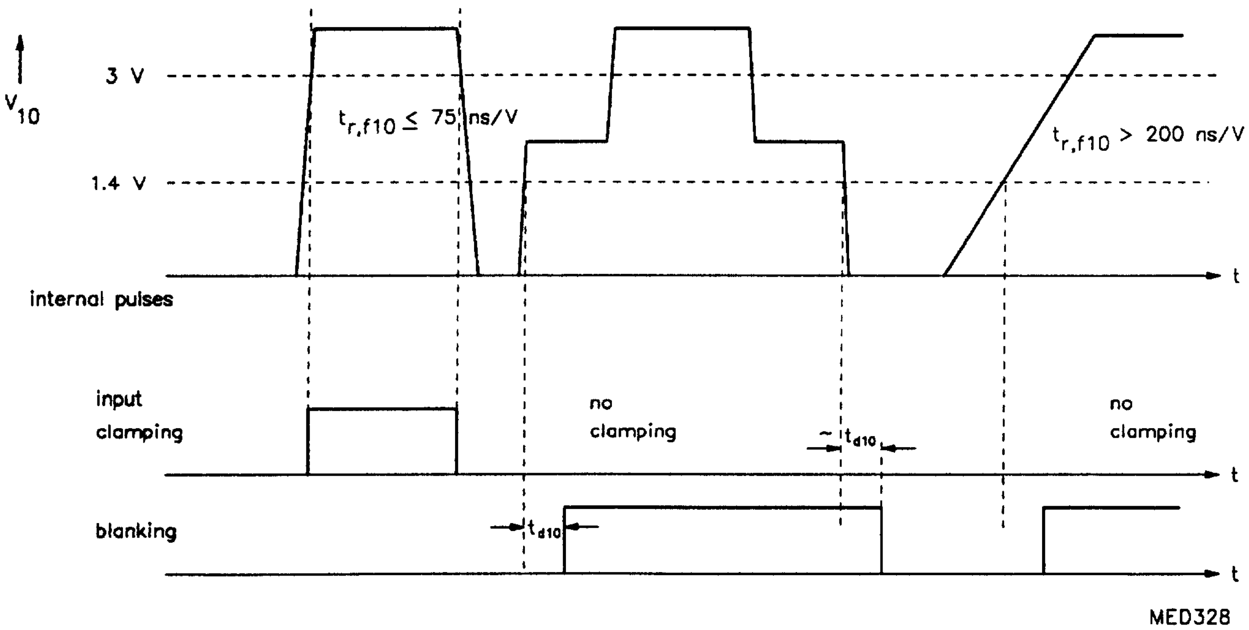
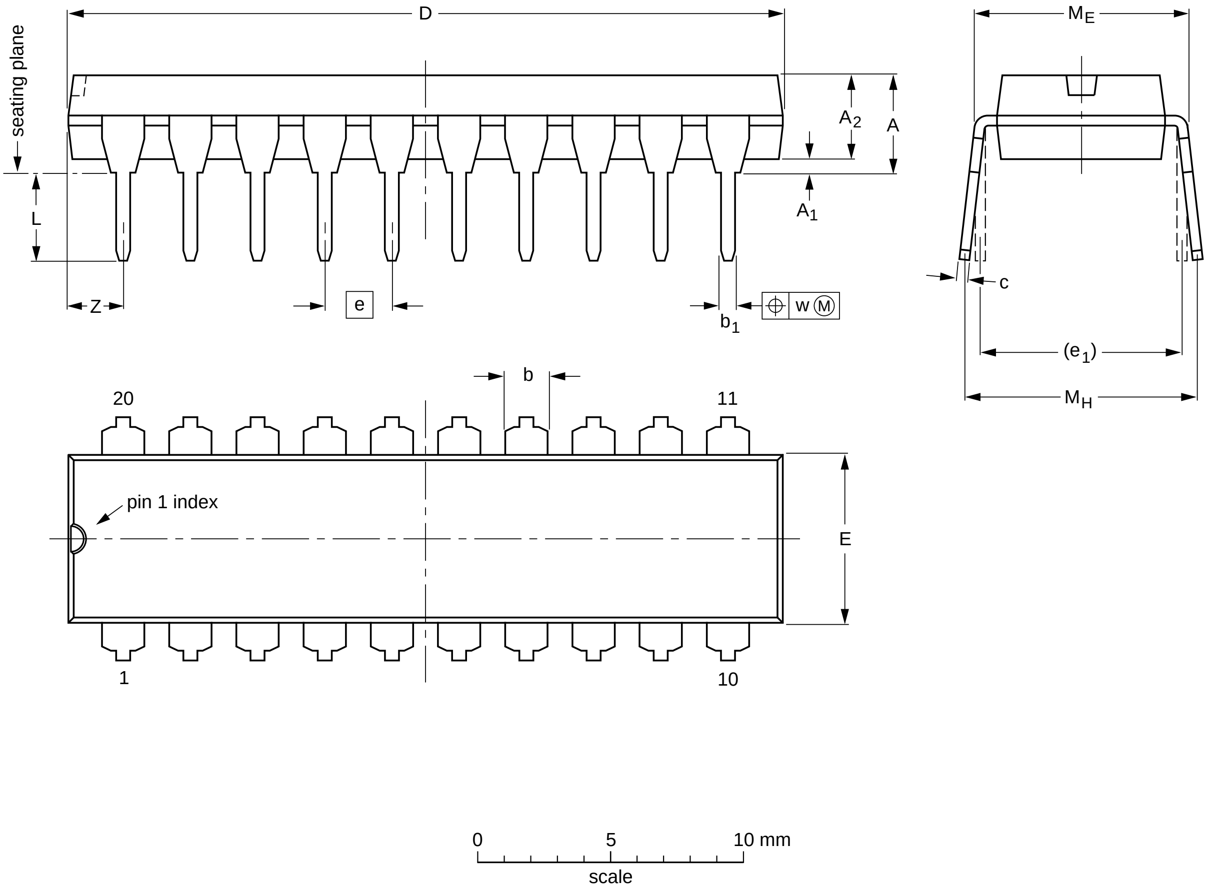


Fig.4 Timing of pulses at pin 10.

PACKAGE OUTLINE

DIP20: plastic dual in-line package; 20 leads (300 mil) **SOT146-1**

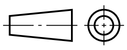


DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	0.36 0.23	26.92 26.54	6.40 6.22	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.0
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.014 0.009	1.060 1.045	0.25 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.078

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT146-1			SC603			~~92-11-17~~ 95-05-24

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Soldering by dipping or by wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.